CBCS SCHEME

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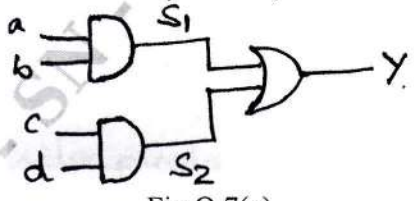
BEC302

Third Semester B.E./B.Tech. Degree Examination, June/July 2024
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Define combinational logic. Give two examples.	4	L1	CO1
	b.	Explain the procedure to place a sum of products equation into canonical form. Express the function P = f(a, b, c) = ab′ + ac′ + bc in canonical form.	6	L2	CO1
	c.	Solve the function K = f(w, x, y, z) = Σ(0, 1, 4, 5, 9, 11, 13, 15) using Karnaugh map.	4	L2	CO1
	d.	Simplify the function F = f(P, Q, R, S) = Σm (0, 3, 5, 6, 7, 11, 14) using Quine-McCluskey method.	6	L2	CO1
		OR			
Q.2	a.	Define canonical sum of products and canonical product of sums. Give examples.	4	L1	CO1
	b.	Explain the procedure to place a product of sums equation into canonical form. Explain the function T = f(a, b, c) = (a + b′) (b′ + c) in canonical form.	6	L2	CO1
	c.	Solve the function G = f(a, b, c, d) = π(0, 4, 5, 7, 8, 9, 11, 12, 13, 15) using Karnaugh map.	4	L2	CO1
	d.	Simplify the function F = f(P, Q, R, S) = Σm(1, 2, 3, 5, 9, 10, 12) using Quine-McCluskey method.	6	L2	CO1
		Module – 2			
Q.3	a.	Define encoder. Write the truth table, equations and circuit diagram of 8 – to – 3 – line priority encoder.	4	L1	CO2
	b.	Explain the concept of carry-lookahead adder with related equations and block diagram.	6	L2	CO2
	c.	Design one-bit comparator with inputs A_i, B_i – bits to be compared, G_i, E_i, L_i – previous stage inputs and with the outputs G_{i+1}, E_{i+1}, L_{i+1}.	6	L4	CO2
	d.	Implement the function f(w, x, y, z) = Σm(0, 1, 5, 6, 7, 9, 12, 15) using 8 – to – 1 – line multiplexer.	4	L3	CO2

		OR			
Q.4	**a.**	Define decoder. Write the truth table, equations and circuit diagram of 3 – to – 8 – line decoder.	**4**	**L1**	**CO2**
	b.	Explain the operation of 8 – to – 1 line multiplexer with block diagram, truth table, equation.	**6**	**L2**	**CO2**
	c.	Construct parallel binary adder/subtractor using full adder block and EX-OR gates. Also explain the operation of it.	**6**	**L3**	**CO2**
	d.	Design two-bit comparator using cascade connection of one-bit comparators and explain its operation.	**4**	**L4**	**CO2**
		Module – 3			
Q.5	**a.**	State transparency property in latches. What is the need for master-slave flip flops?	**4**	**L1**	**CO3**
	b.	With neat block diagram and truth-table explain the operation of master-slave JK flipflop.	**6**	**L2**	**CO3**
	c.	Design a synchronous mod-6 counter using JK flipflops.	**6**	**L4**	**CO3**
	d.	Implement mod-4-ring counter using shift registers.	**4**	**L3**	**CO3**
		OR			
Q.6	**a.**	Define register and shift register. Mention two applications of shift registers.	**4**	**L1**	**CO3**
	b.	With logic diagram and timing diagram explain the operation of positive edge triggered D-flip flop.	**6**	**L2**	**CO3**
	c.	Design a four-bit binary ripple up-counter with logic diagram and counting sequence and briefly explain its operation.	**6**	**L4**	**CO3**
	d.	Implement Mod-8 twisted ring counter using shift registers and write the count sequence.	**4**	**L3**	**CO3**
		Module – 4			
Q.7	**a.**	List the different relational operators available in verilog language.	**4**	**L1**	**CO4**
	b.	Explain different verilog data types with examples.	**6**	**L2**	**CO4**
	c.	For the circuit diagram shown in Fig.Q.7(c), develop a verilog program for the output Y in: i) data flow description ii) behavioral description.  Fig.Q.7(c)	**6**	**L3**	**CO4**

	d.	Develop a verilog program to implement 2 × 1 multiplexer using conditional operator. Also write the truth table of 2 × 1 multiplexer.	4	L4	CO4
		OR			
Q.8	a.	List the different styles of descriptions in verilog programming.	4	L1	CO4
	b.	Explain verilog shift operators and arithmetic shift operators with examples.	6	L2	CO4
	c.	Let A = 5'b11011, B = 5'b10101, C = 4'd3. Determine the output of the following verilog program statements: i) d = &A ii) e = ~^ 4'b1011 iii) f = ~(A & (~B)) iv) g = A||B v) b = 3 ** 2 vi) i = {2{A}}.	6	L3	CO4
	d.	Develop a verilog program for half subtractor using data flow description style by providing truth table and expressions.	4	L4	CO4
		Module – 5			
Q.9	a.	Write the verilog format of if-else statement and explain it.	4	L1	CO4
	b.	Explain the operation of positive triggered JK flipflop by writing verilog code using case statement and truth table.	6	L2	CO4
	c.	Develop a verilog behavioral description code for calculating the factorial of positive integers.	6	L3	CO4
	d.	Develop a verilog program for D-latch using behavioral description style by providing truth table.	4	L4	CO4
		OR			
Q.10	a.	Write the verilog format of case statement and explain it.	4	L1	CO4
	b.	Explain the operation of 2-to-1-line multiplexer by writing verilog structural description program and block diagram.	6	L2	CO4
	c.	Develop a verilog behavioral description code for three-bit binary up counter.	6	L3	CO4
	d.	Develop a verilog program for half adder using structural description style by providing truth table and expressions.	4	L4	CO4

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